APPARATUS AND METHOD FOR ERROR DETECTION ON SOURCE-SYNCHRONOUS BUSES

ABSTRACT

One embodiment of the present invention provides a system for detecting errors on a source-synchronous bus. The source-synchronous bus includes a plurality of data lines and a clock line. A transmitting mechanism configured to transmit data on the source-synchronous bus is coupled to the source-synchronous bus. A receiving mechanism configured to receive data from the source-synchronous bus is also coupled to the source-synchronous bus. An error detecting mechanism configured to detect errors on the source-synchronous bus is coupled to the receiving mechanism. The error detecting mechanism can detect errors on the plurality of data lines including errors that are caused by an error on the clock line.